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Band alignment and defect states at SiC/oxide interfaces

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Abstract

Comparative analysis of the electronic structure of thermally oxidized surfaces of silicon and silicon carbide indicates that in both cases the fundamental (bulk-band-related) spectrum of electron states is established within less than 1 nm distance from the interface plane. The latter suggests an abrupt transition from semiconductor to insulator. However, a large density of interface traps is observed in the oxidized SiC, which are mostly related to the clustering of elemental carbon during oxide growth and to the presence of defects in the near-interfacial oxides. Recent advancements in reducing the adverse effect of these traps suggest that the SiC oxidation technology has not reached its limits yet and fabrication of functional SiC/oxide interfaces is possible.

1. Introduction

The high density of imperfections occurring after oxidation at silicon carbide (SiC)/oxide interfaces represents a serious obstacle in the development of functional metal–oxide–semiconductor (MOS) devices on SiC [1–3]. After nearly a decade of intensive research efforts in the field of SiC oxidation, it remains unclear what factor(s) make(s) the interface between thermal oxides and SiC so dramatically different from the 'classic' and highly successful SiO_2/Si interface. In this respect, one may note, for instance, that the Si face of hexagonal SiC polytypes of (0001) surface plane is structurally isomorphic with the (111) Si surface. However, oxidation of these two surfaces, after additional passivation treatments, results in interfaces with densities of electrically active centres different by at least two orders of magnitude, i.e., of the order of 10^{10} cm^{-2} in Si/SiO_2 [4] and 10^{12} cm^{-2} in SiC/SiO_2 [5]. The major question, still unanswered, is whether this high density of structural imperfections (leading to the high interface trap density) is an *intrinsic property* of the oxidized SiC or not. Depending on the answer, one should either discontinue the technological application of SiO_2 growth through

Table 1. Conduction and valence band offsets, ΔE_c and ΔE_v, at the interfaces between Si and SiC with different oxide insulators. (Bold numbers indicate experimental band-gap and band-offset values determined by internal photoemission spectroscopy.)

Insulator	SiO_2	Al_2O_3	ZrO_2	HfO_2
E_g (eV)	**8.9**	**6.2**	**5.4**	**5.6/5.9**
Semiconductor	$\Delta E_c/\Delta E_v$ (eV)	$\Delta E_c/\Delta E_v$ (eV)	$\Delta E_c/\Delta E_v$ (eV)	$\Delta E_c/\Delta E_v$ (eV)
Si	**3.1/4.7**	**2.1**/3.0	**2.0**/2.3	**2.0/2.5**
3C-SiC	**3.6**/2.9	2.6/1.2	2.5/0.5	2.5/0.7
15R-SiC	**3.0**/2.9	2.0/1.2	1.9/0.5	1.9/0.7
6H-SiC	**2.95/2.9**	1.95/1.2	1.85/0.5	1.85/0.7
4H-SiC	**2.7/2.9**	1.7/1.2	1.6/0.5	1.6/0.7

thermal oxidation of SiC, and look for another, alternative insulating material, or continue with, if not intensify, the efforts to optimize SiC oxidation, aiming at the reduction of interface imperfections.

Yet there exists no consensus regarding this subject. On the one hand, the theoretical results suggest that the topology and geometry of SiC surfaces are not suitable for abrupt interfaces [6, 7]. This would make suboxide bonds inevitable, leading to a graded SiC–oxide transition with poor insulating properties. Moreover, it has been suggested that even in the absence of extrinsic contributions to the SiC/SiO_2 interface trap density, there will arise intrinsic states due to the perturbation of the SiC valence band states at the interface [8]. On the other hand, the experimental results reveal a clear trend of gradual improvement of the SiC/SiO_2 interface electrical properties as better (alternative) procedures are employed for SiC epitaxial layer growth, pre-oxidation surface preparation, oxidation parameters, and the post-oxidation treatment. This continuing trend suggests that there is still room for further improvement. In other words, the theoretically predicted fundamental limits seem not to be reached yet, and it may be possible to realize functional SiC MOS devices using SiC/SiO_2.

The goal of the present paper is to summarize the available experimental results concerning electron states at the oxidized SiC surfaces in order to evaluate the room left for possible improvements. Alternative approaches to insulator formation on SiC, other than SiC/oxide through thermal oxidation, will also be discussed.

2. Band offsets at SiC/SiO_2 interfaces

At the interface the spectrum of electron states related to the fundamental bulk energy bands of the semiconductor and the insulator can be characterized in a most straightforward way through the determination of conduction and valence band offsets. These values are pertinent to the question of how abrupt the transition from one solid to another is, and whether or not an additional phase with different electronic spectrum is present at the interface. Therefore, the available information on SiC/insulator band offsets will be discussed in this section.

2.1. Conduction band offsets

Experimental determinations of the conduction band offset at the interface are usually based on observations of electron emission (injection) from the semiconductor into the insulator. The most straightforward method consists of the analysis of spectral curves of internal electron photoemission (IPE) in which the barrier height for electrons is defined as the spectral threshold of IPE [9, 10]. (See figure 1(a) for a sketch of the basic IPE processes and determination of pertinent parameters.) Although this method is demanding from the point of view of experimental arrangements, the interpretation only needs a minimal set

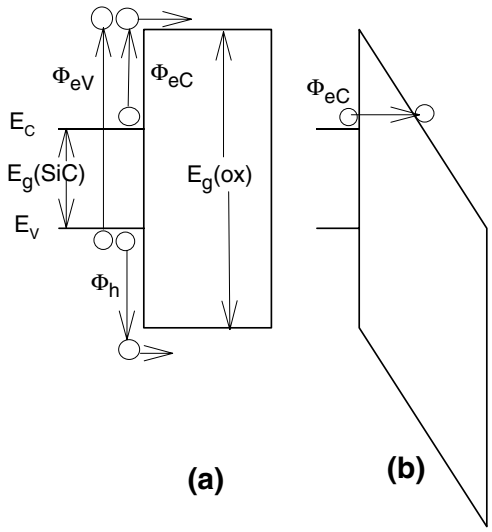

Figure 1. Band diagrams outlining the energy barriers and band parameters pertinent to the optically excited (a) and dark (b) electron transitions corresponding to the electron IPE from the semiconductor conduction (Φ_{eC}) and valence (Φ_{eV}) bands, the hole IPE from the valence band (Φ_h), and the electron tunnelling from the conduction band (Φ_{eC}). The band gaps of the semiconductor and insulator are indicated also.

of assumptions, which allows one to avoid systematic errors. The IPE technique has been successfully applied to determine the electron energy barriers at the interfaces between four SiC polytypes (3C-, 15R-, 6H-, 4H-SiC), and thermally grown SiO_2 layers [10]. The results concerning the conduction band offset (ΔE_c) are summarized in the first column of table 1. It is worth mentioning here that IPE from both the valence and conduction bands of SiC was observed, which allows one to determine the energy position of each of the bands at the interface. It appears that in all four SiC polytypes the top of valence band lies at $\Phi_{eV} = 6.0 \pm 0.1$ eV below the conduction band of SiO_2, while the conduction band edge shifts in accordance with the SiC polytype band-gap width variation as indicated in table 1.

The barrier values show little sensitivity to the thickness of the oxide grown. As studied on n-type 4H-SiC MOS capacitors, this is borne out by the IPE spectra shown in figure 2 for a 20 nm thick SiO_2 on 4H-SiC(0001) as compared to a stack of 3.9 nm SiO_2 with 20 nm of HfO_2 [11]. The latter oxide has a considerably smaller band gap than SiO_2, which yields a lower barrier at the interface with Si [12]. Therefore, the IPE will be governed by the highest barrier, i.e., related to the properties of the ultrathin SiO_2 interlayer which appear to be indistinguishable from those of a thicker oxide. More information can be obtained from the field dependence of the IPE spectral threshold. Its value corresponds to the image-force potential barrier maximum in the oxide, which shifts closer to the emitter surface with increasing strength of the applied electric field [13]. The threshold energy position corresponds to the insulator conduction band edge at this distance, corrected for the Schottky effect. This property can be used to trace the possible occurrence of a graded transition region or an interfacial phase with a conduction band position different from that in the bulk of the insulator. In this way it was found that the SiO_2 conduction band edge has already attained its bulk position at the Si/SiO_2 interface at the distance of 0.4 nm from the Si surface [14]. Using the same method, from the Schottky-type barrier reduction observed at the SiC/SiO_2 interfaces (see figure 6 in [10]) one can derive that the oxide conduction band energy reaches the value corresponding to that of stoichiometric SiO_2 within a distance of 0.5 nm. The latter corresponds to the highest strength of electric field (6.4 MV cm^{-1} for 6H-SiC/SiO_2) attained in the IPE experiments and sets an upper limit of the transition layer thickness.

Another method of barrier characterization makes use of electron tunnelling between the conduction bands of the semiconductor and the insulator, as shown in figure 1(b). Within the

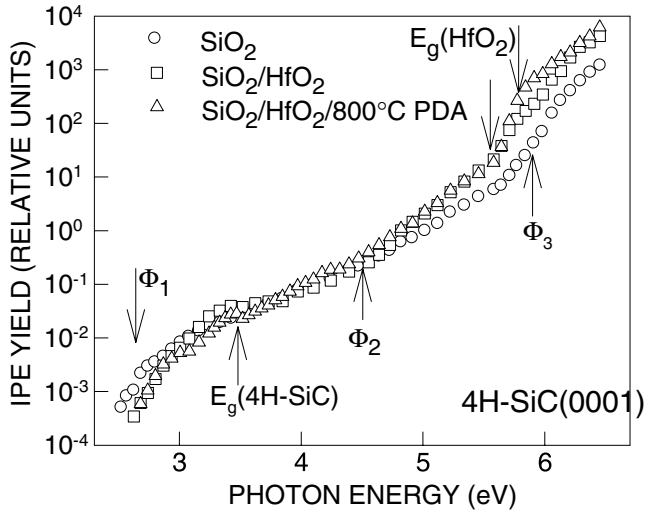

Figure 2. IPE spectra measured for n-type 4H-SiC MOS capacitors with different insulators: 20 nm thick thermal SiO_2(O), a stack of SiO_2 (3.9 nm)/HfO_2 (20 nm) (□), and the latter stack after 10 min PDA at 800 °C in 5%O_2 + N_2 (△). The spectra are measured under +3 V bias on the metal (gold) electrode. The IPE yield is defined in terms of photocurrent normalized to the incident photon flux. The arrows Φ_1, Φ_3 indicate the thresholds from conduction and valence bands of SiC, respectively. The threshold Φ_2 is related to excitation of SiC/SiO_2 interface defects. The band gaps of 4H-SiC and HfO_2 (two values, see table 1) are also indicated.

framework of the Fowler–Nordheim model the tunnelling current depends exponentially on the barrier height, which can be determined by proper analysis from the tunnelling data provided that the effective electron mass (m_e^*) in the oxide is known [15, 16]. The latter requirement results in a considerable uncertainty because direct experimental determination of m^* in a wide-band-gap solid is not always possible. However, in the case of SiC/SiO_2 interfaces one can use the same m_e^* as in the much better studied Si/SiO_2 system [16], thus improving the reliability of the analysis. An important feature of the tunnelling current method consists in the dominant (exponential) contribution to the measured current of interface regions with the *lowest barrier*. Thus, if the tunnelling rate is locally enhanced by some defects present in the oxide or by local shrinking of its band gap, the barrier height derived from the tunnelling current analysis will be lower than that derived from the IPE. In addition, if a transition layer of any substantial width were to be present at the interface between the semiconductor and the insulator, it would strongly affect the tunnelling measurements which are usually performed at high electric field strength. By contrast, the impact of barrier nonuniformity on the IPE process will be marginal because the electron escape probability depends linearly on the normal component of its kinetic energy [9, 13]. Thus, by comparing the barriers determined by means of IPE and by tunnelling, one may infer information regarding the abruptness of the interface.

The barrier heights measured at room temperature using the electron tunnelling method appear to depend significantly on the way in which one interprets the current–voltage curves: for substrates of the same SiC polytypes, barriers differing by more than 0.5 eV were reported from applying different procedures of analysis [17–20]. Nevertheless, the reported values are still not far from the SiC/SiO_2 conduction band-offset values determined by means of IPE. Importantly, this indicates that, from the point of view of electron transport, one may consider SiC/SiO_2 interfaces as abrupt. The reduction in the tunnelling barrier height observed in the SiC MOS structures at elevated temperatures can be successfully explained by an enhanced

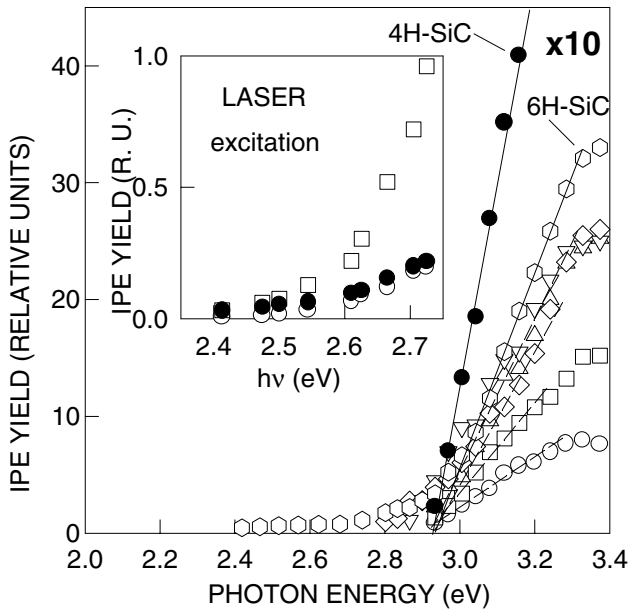

Figure 3. Hole IPE yield as a function of photon energy for a p^+-type 6H-SiC MOS structure ($n_a \approx 10^{18}$ cm^{-3}) with a 100 nm thick oxide at different electric field strengths in the oxide (in MV cm^{-1}): 0.5 (○), 1 (□), 2 (◇), 3 (△), 4 (▽), and 5 (⬡). The IPE yield for the p-type 4H-SiC MOS structure ($n_a = 4 \times 10^{16}$ cm^{-3}) with 100 nm thick oxide is shown for oxide field of 4 MV cm^{-1} (●). The inset shows the spectral curves measured under laser excitation with an applied oxide field of 4 MV cm^{-1} in p-type 6H-SiC ($n_a = 4 \times 10^{16}$ cm^{-3}) (○), p-type 4H-SiC ($n_a = 4 \times 10^{16}$ cm^{-3}) (●), and p^+-type 6H-SiC ($n_a \approx 10^{18}$ cm^{-3}) (□) MOS structures. The lines guide the eye.

tunnelling rate resulting from the high-energy tail of the electron distribution in the SiC conduction band [18–20].

2.2. Valence band offsets

In the case of solid/solid interfaces one can not only observe IPE and tunnelling of *electrons* but also that of *holes* [9]. Both these effects are observed at the SiC/SiO_2 interfaces, thus allowing direct determination of the valence band offset. The hole IPE spectra shown in figure 3 for 6H- and 4H-SiC/SiO_2 interfaces indicate for each the same valence band offset of 2.9 ± 0.1 eV [21]. The interpretation of the hole tunnelling appears to be less straightforward because the effective mass of holes in SiO_2 (m_h^*) is unknown. When using a tunnelling barrier height that is the same as the IPE threshold [22, 23], one arrives at unrealistically low m_h^*-values, i.e., in the range of 0.2–0.5 times the free electron mass (m_0), as compared to the theoretical estimate of $m_h^* = 5$–$10\ m_0$ [24]. Analysis of the photon-stimulated hole tunnelling suggests that this discrepancy may be due to the defect-assisted hole injection process involving traps energetically located at ∼1 eV above the Si-oxide valence band [21]. The IPE spectra taken using laser excitation reveal this injection mechanism, as shown in the inset in figure 3. The oxide states in the same energy range are also observed in oxidized Si from both hole IPE and photoconductivity measurements [9, 25]. Their observation in SiC/SiO_2 as well suggests these traps to be related to some intrinsic oxide defects.

Another method of the valence band-offset determination uses external photoelectron emission from the valence states of the SiC substrate and a thin SiO_2 overlayer. These mea-

surements gave a value ∼1 eV smaller than the IPE ones [26]. This difference, however, is likely to be associated with the oxygen plasma treatment of the SiC surface used to grow SiO_2: one can note from table 2 in [26] that the plasma exposure shifts the SiC valence band maximum by 0.7–0.9 eV down with respect to the case of the same surface exposed to O_2 gas. So, were the latter to be used as the reference, the band offsets would agree with the IPE results within the experimental error. It is likely that the plasma exposure leads to formation of the negative charge at the oxide surface. This may be related, for instance, to the adsorption of O_2^- ions at the oxide surface known to occur in Si/SiO_2 [27]. The latter would not only explain the shift of the SiC valence band with respect to the Fermi level of the electron energy analyser, but also the attendant observed difference in the Si 2p core level position as compared to other works [28–31] and a band bending in SiC which would correspond to an unrealistically high interface state density.

2.3. Band-gap width at the interface

The above-described barrier height measurements allow evaluation of the band-gap width for both the semiconductor and the insulator in the probed interface region [9, 21, 25]. The thickness of the latter from the semiconductor side is of the order of the mean free path of excited photoelectrons (≈1 nm for Si; see [32]), while the insulator probing depth can be estimated as the distance between the emitter surface and the maximum of the image-force potential barrier as discussed in section 2.1. The semiconductor band-gap width can be obtained directly as the difference between the thresholds of the electron IPE from the valence and conduction bands. This value appears to coincide with the optical band-gap width in all four SiC polytypes studied (3C, 15R, 6H, 4H) [10], importantly indicating the absence of any detectable oxidation-induced polytype transformation at the surface of SiC. This conclusion is further corroborated by the recent observation that the intensity of the energy loss feature in the electron IPE spectra corresponding to the onset of electron–electron scattering in 4H-SiC remains unaffected by the oxidation temperature [33]. Therefore, at least in the case of thermal oxidation of SiC, one can still use the bulk SiC band-gap value for the SiC/oxide interface.

With this knowledge to hand, one can further combine the valence and conduction band offsets to obtain the insulator band-gap width as $E_g(\mathrm{ox}) = \Delta E_C + \Delta E_V + E_g(\mathrm{SiC})$, which is evident from figure 1(a). Moreover, as regards SiC, the energy barrier between the SiC valence band and the conduction band of the oxide can simply be added to the valence band offset yielding $E_g(\mathrm{ox}) = 8.9 \pm 0.15$ eV. The latter value coincides with the band gap of oxide thermally grown on Si as determined from the photoconductivity (the bulk value) [9, 34] and the electron/hole IPE (the interface value) [9, 25] measurements. Thus, from the point of view of the fundamental electron state spectrum, there are no indications that oxidation of SiC results in an interface of a graded type; i.e., the SiC/SiO_2 transition appears as abrupt as the Si/SiO_2 one.

2.4. Band offsets at the interfaces of SiC with alternative insulators

Despite the attractive properties and versatility linked with using the native oxide as the MOS insulator, there is considerable interest in the search for alternative insulating materials on SiC. This is primarily related to the problems associated with the application of SiO_2 at high temperatures and high electric fields: silicon dioxide in both cases exhibits an accelerated degradation [35–37], thus limiting its advantages in SiC MOS applications. As a possible solution of the insulator reliability problems, an alternative, more stable insulator is investigated. From the point of view of high thermal stability, several aluminium compounds, including Al oxide, nitride, and oxynitride, have been considered [38–42]. Although reasonable insulating properties were observed in the case of positive bias applied to MOS

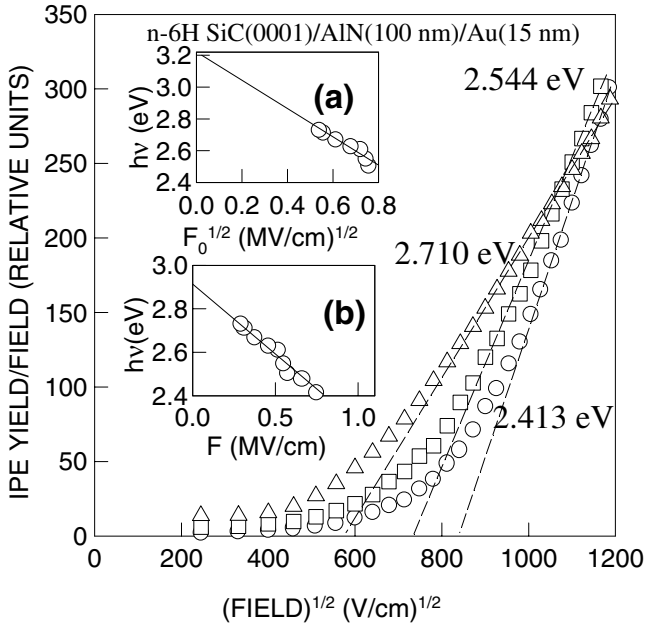

Figure 4. Photocurrent as a function of electric field in an (0001) 6H-SiC/AlN/Au capacitor under laser excitation for different photon energies. The insets illustrate the interface barrier height determination within the framework (a) of the Schottky barrier reduction model [13] or (b) assuming electron excitation from a trap in the insulator [9].

capacitors, the leakage current appears to be unacceptably high in the case of negative bias applied to the p-type SiC MOS structures, suggesting a low barrier for holes in SiC in such structures. With the band-gap width of both AlN [43, 44] and the low-temperature-grown amorphous alumina [45] only slightly exceeding 6 eV, its asymmetric position with respect to the SiC band gap is the most probable reason for the high leakage current under one polarity of the applied bias.

The direct barrier measurement here by means of IPE is hindered by high leakage currents, which necessitates the use of high-intensity laser excitation to obtain a reliable photocurrent read-out. In order to overcome the limited spectral range of the Ar^+ ion laser tuning, photocurrent–voltage measurements were performed at each available laser wavelength [46]. The curves were then analysed using Powell's method [13] to estimate the conduction band offset at the (0001) 6H-SiC/AlN interface. The procedure is illustrated in figure 4 which, in relative units, shows the IPE yield (Y) normalized to the applied electric field (F) as a function of $F^{1/2}$. The threshold strength of the electric field at which the IPE starts to become observable is plotted in inset (a) for different excitation photon energies. Its extrapolation to zero field yields the barrier height of 3.2 ± 0.1 eV. However, one may also interpret using another model in which the photocurrent is considered as caused by excitation of electrons out of traps in the insulator shifted by the applied electric field below the Fermi level in the semiconductor [9]. Then, one obtains a lower barrier of 2.9 ± 0.1 eV, as illustrated in inset (b). Taking into account that capacitance–voltage measurements indicate a considerable density of negative charge in AlN, the last model would seem to be more realistic. Therefore, one might estimate the conduction band offset between 6H-SiC and AlN to be around 3 eV. This value together with the band-gap widths of 6H-SiC (3.05 eV) and AlN (6–6.2 eV) suggests that the valence band offset at this interface is only few tens of electron volts high.

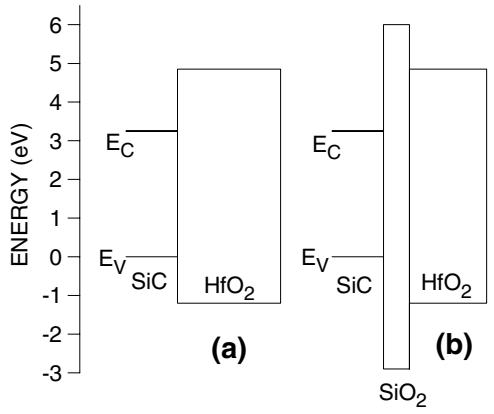

Figure 5. Energy band diagrams of the 4H-SiC/HfO_2 (a) and 4H-SiC/SiO_2/HfO_2 (b) structures as evaluated from IPE experiments at the SiC/SiO_2, Si/SiO_2, and Si/HfO_2 interfaces. The zero of the energy scale is at the silicon carbide valence band top.

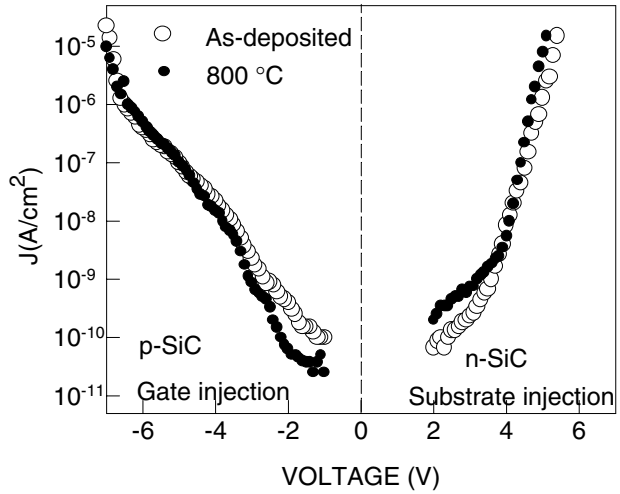

Figure 6. *I–V* curves for n- and p-type 4H-SiC MOS capacitors with an insulating stack of 3 nm SiO_2 and 20 nm HfO_2 without (○) and with (●) 10 min PDA at 800 °C in 5% $O_2 + N_2$ (1 atm).

More detailed information regarding the relative energy position of bands for the interfaces between SiC and metal oxide insulators can be obtained by combining the experimental data for the Si and SiC interfaces with the native SiO_2 [10] and the IPE barrier heights recently published for the Si/metal oxide interfaces [12, 47]. This is allowed because the dipole contributions to the barrier heights were found to be negligible [48], both for interfaces of various SiC polytypes with SiO_2, and for the interfaces of Si with metal oxides: for instance, the conduction band offset at the interfaces of Si with HfO_2 shows no measurable dependence on either the type of interlayer between the semiconductor and the insulator (SiO_2, SiON, or Si_3N_4) or the subsequent thermal treatment [12]. Therefore, the band offsets can be calculated using the energy of the SiO_2 band-gap edges as the reference levels. The results are summarized in table 1 for Si, four SiC polytypes for which the band offsets at the interface with SiO_2 are known, and four insulating materials: SiO_2, Al_2O_3, ZrO_2, and HfO_2. It is seen that the valence band offsets for all three metal oxides are much reduced as compared to SiO_2, thus resulting in a low barrier height for holes in SiC which may potentially cause high leakage current.

As a possible solution one might combine an ultrathin SiO_2 layer with a thicker metal oxide as depicted in figure 5. While this kind of insulating stack is unlikely to provide substantial advantages for high-temperature SiC MOS devices, it may allow application of a high electric

field to the SiC surface needed to fully employ the advantages provided by the high value of the electron saturation velocity in SiC. This approach was recently tested on 4H-SiC/HfO_2 structures and suggests that significant improvement of electrical properties can be achieved in MOS structures with a thin SiO_2 interlayer [11]. For example, a substantial reduction in leakage current is attained when a 3 nm thick SiO_2 is incorporated as an interlayer between 4H-SiC and HfO_2, as shown in figure 6. Also shown in that figure are data taken after applying post-deposition annealing (PDA) at 800 °C in 5% O_2 + N_2. Clearly, this indicates that the insulating stack has sufficient thermal stability to enable the use of conventional polycrystalline silicon gate technology.

3. SiC/oxide interface imperfections

The character of the SiC–oxide transition revealed by the bulk band-related electron spectrum of SiC/SiO_2 interfaces suggests that it does not differ drastically from that of classical Si/SiO_2 and, therefore, cannot account for the significantly higher defect density found in the SiC/SiO_2 structure. More likely is that interface imperfections are the most probable cause for the enhanced SiC/SiO_2 interface state density (D_{it}) and inferior (as compared to Si/SiO_2) electrical properties. In this section we will review the general properties of the SiC/SiO_2 interface state spectrum and pertinent interpretive atomic models.

3.1. Energy distribution of SiC/SiO_2 interface states

The analysis of the energy distribution of interface states may provide important information on the nature of the interfacial region between the semiconductor and insulator. In the case of interface disorder one might expect that the imperfections, e.g., the dangling bond centres, will be imbedded in a strained surrounding with chemical composition different from that of the substrate and oxide overlayer. This would lead to a broad energy spectrum or even to a continuum of interface states as is generally observed in amorphous semiconductors. On the other hand, if the transition were abrupt the imperfections would find themselves in well-defined (crystalline) surroundings leading, in turn, to well-defined electron configurations. The latter are characterized by electron binding energies confined to a narrow interval and yielding peaks in D_{it}. This is observed, for instance, at the interfaces of silicon with thermal oxide [49].

To analyse D_{it} across the entire SiC band gap one may combine the electrical data on n- and p-type MOS capacitors obtained from capacitance and ac conductance–voltage measurements at different temperatures. Some results are shown in figure 7 as the energy distributions of D_{it} at the interfaces between the Si faces of three polytypes of SiC (3C-, 6H-, and 4H-SiC, of both n- and p-type conductivity) with SiO_2 thermally grown in dry O_2 [5]. They reveal two effects, which may possibly account for the higher interface state density observed in the oxidized SiC as compared to Si. First, as the band gap of SiC is two (in 3C-SiC) to three (in 4H-SiC) times [50] wider than that of Si, there may occur, as compared to the Si case, additional energy levels falling within the semiconductor band gap that can be re-charged when sweeping the Fermi level in SiC, i.e., which will act as interface traps. This is indeed the case, as evidenced in figure 7: the regions with highest D_{it} lie outside the Si band-gap energy window. Second, the defects in the oxidized SiC appear to be much more numerous than in passivated (111) Si/SiO_2 ($\approx 10^{10}$ cm^{-2} eV^{-1}) even when considering only the narrow spectral range spanned by the Si band gap, with a considerable difference between the three SiC polytypes studied.

The high density of SiC/SiO_2 interface states is also revealed by IPE spectroscopy [5, 10]: in addition to the IPE thresholds related to emission of electrons from the conduction and valence bands of SiC, marked as Φ_1 and Φ_3 in figure 2, respectively, there appears an additional threshold Φ_2 between them, corresponding to an energy range within the band gap for both

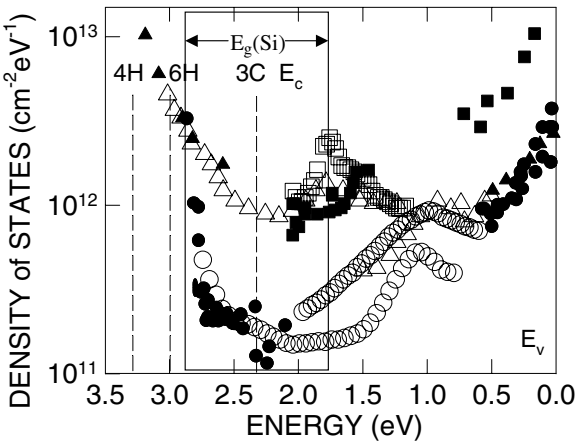

Figure 7. Interface state density D_{it} as a function of energy for 3C-SiC/SiO_2 (□, ■), 6H-SiC/SiO_2 (○, ●), and 4H-SiC/SiO_2 (△, ▲) MOS structures determined from admittance spectroscopy (filled symbols) and from constant-capacitance deep-level transient spectroscopy (open symbols). The zero point of the energy scale corresponds to the top of the SiC valence band. The dashed lines indicate the energy position of the conduction band edge for the SiC polytypes investigated; the solid lines mark the edges of the silicon band gap.

SiC and SiO_2. At a defect-free interface there should be no populated electron states in this energy range. Therefore, this IPE is associated with electron states of some imperfections at the interface between SiC and the oxide. These states appear to be observed at the oxidized surfaces of all the oxidized SiC polytypes studied so far, which agrees with the results of electrical measurements presented in figure 7. As already discussed in detail in [5], the energies of these states are close to the portion of the SiC/SiO_2 D_{it}-distribution in the lower part of the semiconductor band gap. This, together with their observed sensitivity to the technology of SiC oxidation/annealing, suggests that the same defects are observed from both IPE and electrical measurements. Most of these electron states exhibit a donor-type behaviour, which accounts for the positive charges often reported for p-type SiC MOS structures.

A high density of interface states is also revealed near the conduction band edge of 4H-SiC and, albeit to a much lesser extent, that of 6H-SiC, by the Hall effect measurements [51], low-temperature capacitance behaviour [52, 53], and photon-stimulated electron tunnelling into SiO_2 [5, 54]. In contrast to the D_{it} in the lower half of the SiC band gap, these states are observed only in the wide-band-gap polytypes of SiC. Apparently then, they cannot be derived from SiC conduction band states as suggested by theory [8] but, rather, have an energy level not immediately related to the SiC electron states. These states exhibit an acceptor-type electrical behaviour and account for negative charges often observed in the n-type 4H-SiC MOS capacitors and transistors.

As can be seen from figure 7, both the donor- and acceptor-type states exhibit a wide energy distribution. Such a spread is untypical for the Si dangling-bond-type defects (P_b centres) representing threefold-coordinated Si atoms at the (111) plane routinely encountered at the (111) Si/SiO_2 interface [54]. The latter exhibit an amphoteric electrical behaviour with (−/0) and (0/+) transition D_{it}-peaks with a width at half height of 0.2–0.3 eV [54, 55]. Another specific feature of P_b centres is their interaction with hydrogen which results in the formation of electrically inactive $Si_3{\equiv}Si{-}H$ structures [56]. This effect, known as *passivation*, is widely used in Si MOS technology to attain interfaces with low D_{it}. Unfortunately, passivation of the SiC/SiO_2 interfaces is observed to occur only after damaging the region by irradiation or

charge injection. Basically, this restores the D_{it} observed after oxide growth, which is much higher than in the Si/SiO_2 structures [37, 57]. Thus, the defects responsible for this high D_{it} appear to be resistant to hydrogen passivation. These features, together with the fact that densities of SiC/SiO_2 interface donors and acceptors do not appear correlated, indicate that one cannot ascribe these defects to the class of simple Si dangling bond centres common for Si/SiO_2 interfaces. Thus, one must look for alternative atomic models of SiC/SiO_2 interface states.

3.2. Models of SiC/SiO_2 interface states

3.2.1. Impurity-related states. In an attempt to explain why many more donor states are detected in the p-type MOS structures than acceptor states in n-type MOS structures on narrow-band-gap 3C-SiC polytypes, it was suggested that aluminium, used as an acceptor dopant in p-type SiC, migrates to the interface and into the oxide, resulting in high D_{it} [58]. However, no improvement is observed on replacing Al with harmless B acceptors [59]. Moreover, no adverse effect of Al is observed in the n-type 6H-SiC MOS structures obtained by overcompensation of the Al-doped p-type SiC into n-type using N^+ ion implantation [60]. Therefore, incorporation of aluminium is unlikely to provide any significant contribution to D_{it} at the SiC–SiO_2 interfaces.

3.2.2. Carbon cluster model. In a search for 'novel' (different) mechanisms of interface state generation in SiC/SiO_2 structures as compared to Si/SiO_2, it was noticed that over the various SiC surfaces studied, a higher D_{it} is systematically encountered on the faces of SiC with a higher density of carbon atoms [5]. In line with this observation, it was found that the application of specific anti-carbon surface-cleaning steps (UV–ozone exposure) may effect a significant reduction in the SiC/SiO_2 D_{it} [61]. Therefore, it was suggested that excess carbon atoms contribute significantly to SiC/SiO_2 interface state generation. Next, the IPE analysis revealed a similarity between the spectrum of electron states in the SiC band gap of SiC/SiO_2 structures and at the interfaces of hydrogenated amorphous carbon (a-C:H) films with SiO_2 [5, 10]. In a-C:H the highest occupied states correspond to the π-bonds of sp^2-hybridized carbon atoms arranged in clusters of different sizes. The size of a π-bonded carbon cluster determines both the position of the upper filled electron states and the π–π^* splitting which corresponds to the optical band-gap width [62]. Therefore, if one assumes formation of carbon clusters of different sizes during oxidation of SiC, they would account for a quasi-continuum spectrum of interface states.

Within the framework of this 'carbon cluster' model the D_{it}-distribution shown in figure 7 can be explained by a combination of the contributions of π-bonded clusters of different sizes. This is schematically shown in figure 8 for small (wide-band-gap) and large (graphite-like) clusters in the energy range corresponding to the band gap of the three most important SiC polytypes (3C, 4H, and 6H). In small clusters the onset of the filled π-states is energetically located at 4.6 eV below the SiO_2 conduction band edge, i.e., 1.4 eV above the SiC valence band. This energy coincides with the onset of a strong increase in D_{it} in the lower half of the SiC band gap (see figure 7). These π-derived electron states are neutral when completely occupied with electrons but will charge positively if emitting an electron, as happens in the p-type SiC samples in which the Fermi level lies below the carbon cluster π-states. Therefore, these states will exhibit the same donor-type electrical behaviour as observed for the SiC/SiO_2 interface defects. The empty states of the small carbon clusters will be energetically located at $\approx$3 eV above the filled π-states, which corresponds to the band-gap width of a-C:H containing small clusters. Consequently, these states appear to lie well above the SiC conduction band edge and will thus not trap any charge.

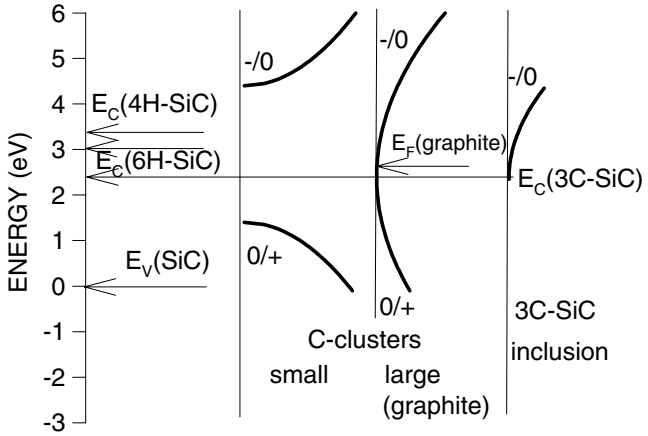

Figure 8. The scheme of the SiC-specific contributions to the interface state density: sp^2-bonded carbon clusters—small and large (graphite-like)—and inclusion of the narrow-band-gap 3C-SiC polytype. The origin of the energy scale is at the SiC valence band top.

With increasing size of an sp^2-bonded carbon cluster, its spectrum of electron states approaches the gapless distribution observed in graphite [62]. From the IPE spectra the Fermi level in graphite is found to be at 3.5 eV below the SiO_2 conduction band, i.e., at $\approx$2.5 eV above the valence band of SiC [63]. The neutrality of the carbon cluster will be preserved only if the Fermi level in SiC coincides with that of graphite. Otherwise the cluster will emit or trap electrons, which would result in positive or negative charge, respectively. Thus, the large carbon clusters represent amphoteric centres with a broad energy distribution spread out over the entire SiC band gap which may account for the continuum of interface states observed in the SiC/SiO_2 D_{it} shown in figure 7. On statistical grounds, however, one may expect the formation of large C clusters to be less probable than generation of small ones. This is considered as the reason that the density of donor states in the lower part of the SiC band gap is higher than in the upper one, in agreement with the experimental results shown in figure 7. Furthermore, within this picture, by ascribing the main D_{it} occurring to the saturated and highly C–C configuration, the carbon cluster model would logically explain the observed stability of SiC/SiO_2 interface traps against passivation with hydrogen.

Since the carbon cluster model was proposed, numerous experimental results appeared in the literature which demonstrate clustering of elemental carbon at the oxidized SiC surfaces and its relationship to the interface state density. Among these we may mention:

- observation of excess carbon at the 6H-SiC/SiO_2 interfaces using angle-resolved x-ray photoelectron spectroscopy and its correlation with D_{it} [64];
- atomic-force microscopy observations of C-related particles after removing thermal oxide from SiC [30, 65];
- transmission electron microscopy/energy loss spectroscopy observation of carbon particles at the SiC/SiO_2 interfaces [66];
- ESR observations of paramagnetic centres related to dangling bonds of C atoms in a surrounding similar to that encountered in amorphous carbon [67, 68].

Thus, the association of the high D_{it} at the SiC/SiO_2 interfaces with carbon clustering appears to be a realistic model, at least for the interface states in the lower part of the SiC band gap.

3.2.3. Oxide defect model. However feasible the carbon cluster model, there is a portion of the SiC/SiO_2 D_{it}-spectrum which cannot be immediately ascribed to the presence of carbon clusters [5]: close to the conduction band of 4H-SiC, D_{it} exceeds 10^{13} cm^{-2} eV^{-1} (according to Hall effect measurements, it approaches 10^{14} cm^{-2} eV^{-1} [51]), which is much higher than observed for the donor states of carbon clusters across the SiC band gap. As a possible explanation, the contribution of intrinsic SiO_2 defects, also observed at the Si/SiO_2 interface [69], was proposed [5]. This suggestion is corroborated by the observation of an uncorrelated variation in D_{it} in the lower part of the 4H-SiC band gap and near its conduction band edge, which points to different atomic origins of the imperfections responsible for these two contributions to D_{it}. Comparative investigations performed both on SiC/SiO_2 and on Si/SiO_2 interfaces suggest that these oxide defects are acceptors characterized by an energy level at $\approx$2.8 eV below the conduction band of SiO_2, i.e., nearly coinciding with the conduction band edge of 4H-SiC. Although the atomic nature of these 2.8 eV traps remains unknown, their density correlates with the presence of excess Si in SiO_2 [70], i.e., they appear associated with an oxygen deficiency centre.

3.2.4. Polytype transformation in SiC. An alternative to the above-outlined oxide defect idea for explaining the high D_{it} near the conduction band of 4H-SiC may entail a local polytypic transition from 4H-SiC to the narrower-gap 3C-SiC polytype. This transition was recently reported upon thermal oxidation of 4H-SiC heavily doped with nitrogen [71]. Were it to occur in the low-doped material normally used for D_{it}-determination, this would lead to a continuum of states in the energy range between the conduction band edges of 4H-SiC and 3C-SiC (see figure 8). There are, however, several results suggesting that no measurable 4H $\rightarrow$ 3C-SiC polytype transition occurs during the normal oxidation procedure. First, the band-gap width of the SiC at the interface with thermal SiO_2 remains that corresponding to the initial SiC polytypes [10], as indicated by the IPE results discussed in section 2.3. Second, no measurable decrease is observed of the 4H-SiC volume fraction at its interface with SiO_2 when the oxidation temperature increases from 1000 to 1300 °C [33], in conflict with what would be expected in the case of thermally activated polytype transformation. In addition, the D_{it} near the SiC conduction band edge does not show a trend of increasing with increasing oxidation temperature either. Finally, the 3C-SiC inclusions formed in 4H-SiC during epitaxial growth have been shown to be responsible for 'fast' interface states [72], while the traps observed in the 4H-SiC MOS structures exhibit large time constants suggesting these traps to be spatially located in the oxide at some distance from the SiC surface plane. Therefore, the adduced available experimental results suggest that the oxide trap model provides a much better account for the observed properties of SiC/SiO_2 interface traps near the SiC conduction band edge than the hypothetical 4H $\rightarrow$ 3C-polytype transformation.

4. Advances in reducing SiC/SiO_2 D_{it}

Recently published experimental results reveal several important trends in reducing D_{it}. These will be discussed in this section in an attempt to demonstrate that the generation of the observed D_{it}-components is not related to fundamentally unavoidable factors. Rather, some experiments suggest that these interface states can potentially be eliminated, thus paving a way to successful SiC MOS device manufacture.

4.1. SiC polytype effect on D_{it}

As silicon carbide comes in a large number of polytypic modifications, one might consider attempting to start from different polytypes in order to improve on D_{it} at the SiC/SiO_2 interfaces.

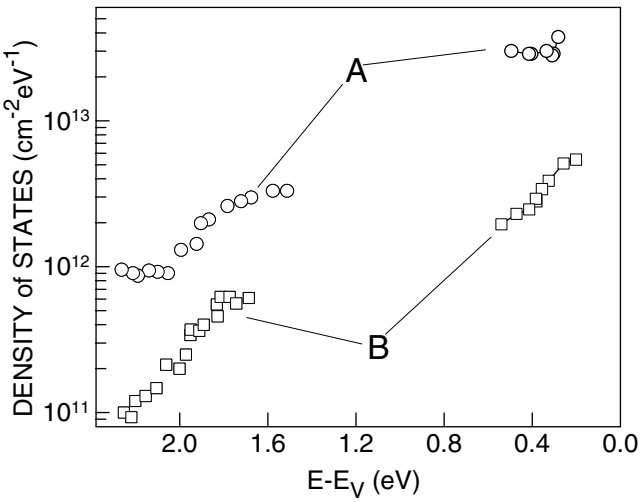

Figure 9. The energy distribution of interface states in (001) 3C-SiC MOS capacitors obtained from ac conductance measurements on samples with Si oxides grown on the substrate crystal in dry O_2 (A) and on the epitaxial SiC layer in pure NO (B).

The early results shown in figure 7 suggest that there are (at least) two basic polytype-related effects [5]: first, there is a polytype-dependent shift in the SiC conduction band edge which might allow one to reduce the impact of the high D_{it} observed near the conduction band of wide-band-gap hexagonal SiC (4H, 6H). Second, there is a substantial impact of the polytype on D_{it} in the central and lower parts of the SiC band gap (see figure 7). The latter effect appears to be strongly sensitive to the quality of the initial SiC epitaxial layer: poor results for 3C-SiC might result from a large density of dislocations as this polytype was initially available only in the form of epitaxial films on Si with ≈20% lattice mismatch. Recently, the homoepitaxial overgrowth of 3C-SiC on free-standing 3C-SiC layers led, after appropriate surface cleaning [73], to much improved results, as demonstrated in figure 9. These results importantly indicate that there is significant room for improving of the 3C-SiC/SiO_2 interface properties through improving the starting material.

More results are currently appearing regarding the behaviour of the interface trap density D_{it} near the conduction band for different SiC polytypes. This is related to the great impact of this portion of the interface state spectrum on the electron mobility in the surface channel of the MOS transistor. When reducing the SiC band-gap width from 4H- to 6H-SiC and further to 15R-SiC (which, due to the fixed valence band position of SiC, corresponds to shifts in the conduction band edge), one observes a systematic improvement in the surface electron mobility [74, 75]. Recently a high mobility value of 180 cm^2 V^{-1} s^{-1} was reported for the even narrower gap of the 3C-SiC device, affirming the above-mentioned trend [76]. The drastic reduction in D_{it} near the conduction band of 3C-SiC is affirmed by the results shown in figure 9 indicating a more-than-tenfold improvement for 3C-SiC as compared to 4H-SiC MOS structures (see figure 7) [73]. The resulting D_{it}, being in the region of 10^{11} cm^{-2} eV^{-1}, approaches the level required for successful MOS devices.

4.2. SiC surface orientation effects

Early results indicated that a considerably higher SiC/SiO_2 interface trap density is typically observed when oxidizing in O_2 the $(000\bar{1})$ surface plane of hexagonal SiC (C face) than when starting from the (0001) plane, which corresponds to the Si face [5, 77, 78]. This was attributed to the generation of a higher density of carbon clusters related to the higher availability of carbon at the surface. This explanation gained additional support from the observation of a

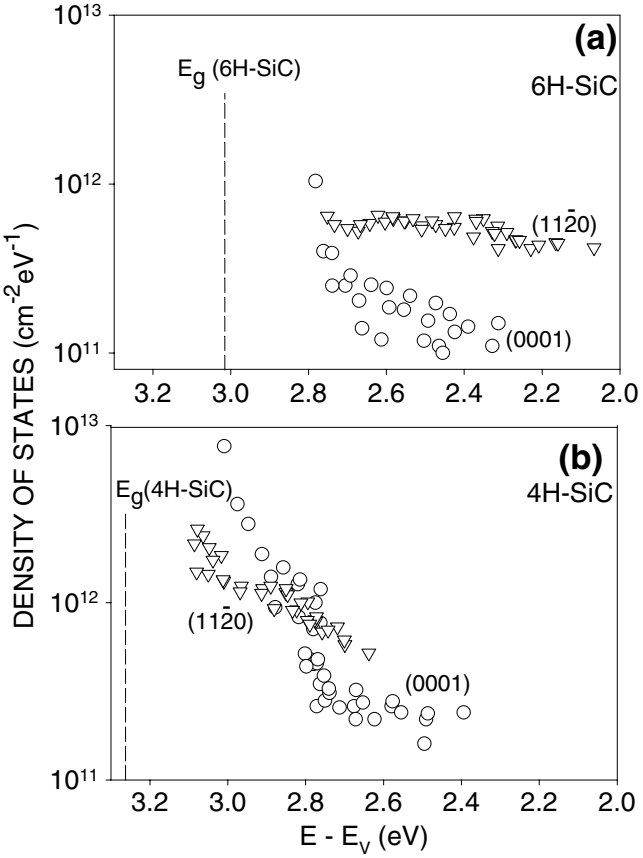

Figure 10. The energy distribution of interface states in SiC MOS capacitors, obtained from ac conductance measurements on samples with oxides grown at 1130 °C in dry O_2 on (0001) (○) and on (11$\bar{2}$0) (▽) faces of 6H-SiC (a) and 4H-SiC (b).

significantly higher D_{it} in the lower part of the SiC band gap in SiC/SiO_2 structures grown on tilted 6H-SiC surfaces [79] and on other surface planes such as (11$\bar{2}$0) and (1$\bar{1}$00) [5, 80, 81].

The behaviour of the SiC/SiO_2 interface states with energy levels close to the SiC conduction band edge appears to be quite different from that of those in the lower half of the SiC band gap. Recent results indicate that the density of interface states at the (11$\bar{2}$0) face of 4H-SiC/SiO_2 is lower than that obtained for growth on the (0001) surface (Si face), suggesting that the traps in the lower and upper parts of the 4H-SiC band gap are of different origin [2, 82]. The D_{it}-distributions obtained using the ac conductance technique for the n-type 6H- and 4H-SiC MOS structures are shown in figures 10(a) and (b), respectively, for two orientations of the SiC surface plane. Interestingly, in 6H-SiC/SiO_2, the D_{it} near the conduction band remains considerably higher for the (11$\bar{2}$0) plane than for the (0001) one, i.e., it correlates with the D_{it} in the lower half of the band gap [82]. Therefore, these could be associated with carbon-related centres, while in 4H-SiC/SiO_2 some additional contribution (probably related to the oxide traps; see section 3.2) appears dominant in this energy range. Also, an improved performance of the (03$\bar{3}$8) plane for 4H-SiC/SiO_2 as compared to the (0001) face has been reported [83]. Taken together, these results suggest the importance of the particular SiC surface atomic geometry for adaptation of the grown-on oxide at the interface. Optimization here may provide significant improvement of electrical properties including electron mobility at the surface of SiC.

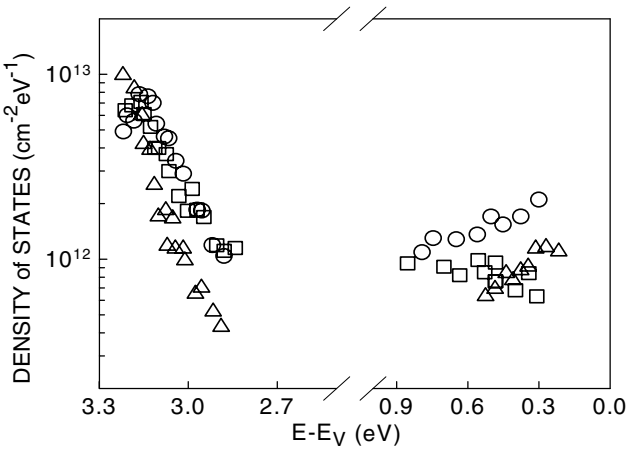

Figure 11. The energy distribution of interface states in 4H-SiC/SiO_2, obtained from ac conductance measurements on samples with oxides grown at 1300 °C in dry O_2 (○) or in 10% N_2O + 90% N_2 (□), and at 1175 °C in NO (△).

4.3. Nitridation of SiC/SiO_2 interfaces

One of the most important recent developments in improving the SiC/SiO_2 interface properties concerns nitridation of the oxide [84]. Nitridation can be carried out either by post-oxidation annealing of the SiC/SiO_2 structures in NO, N_2O, or NH_3, or by direct Si oxide growth in nitric oxide [85–90]. Electrical analysis indicates that a significant reduction of D_{it} can be achieved with such nitrided oxides as compared to the standard dry O_2 oxidation. This is illustrated in figure 11, which shows the 4H-SiC/SiO_2 interface trap density for oxides grown in dry O_2, in a mixture of 10% N_2O + 90% N_2, and in pure NO [91]. These results bear out a significant reduction of D_{it} in the lower part of the 4H-SiC band gap and an even stronger decrease in the interface trap density near the conduction band of 4H-SiC (figure 11). As a result, nitridation will enable a significant improvement in the electron mobility at the oxidized 4H-SiC surfaces [88]. As an additional beneficial aspect, a strong reduction in the injection-induced degradation was reported in the 4H-SiC MOS structures with nitrided oxides [87].

The mechanism of nitrogen impact on SiC/SiO_2 interfaces is likely to be a complex one, as it apparently affects various parts of the D_{it}-distribution of different chemical origins at the same time. A key chemical observation consists in the detection of Si≡N bonds by x-ray photoelectron spectroscopy after N incorporation [86]. These strong bonds can influence both the interfacial oxide structure (as, admittedly, nitrogen allows better accommodation of the interface strain), and the termination of the SiC surface itself. The formation of stable Si≡N bonds at the surface of SiC is suggested by the observation of a greatly reduced oxidation reaction rate, with attendant higher activation energy, importantly indicating a reduced density of reaction sites at the oxidizing surface of the SiC crystal [87]. The reduction in the carbon cluster density, as hinted by the observed reduction in D_{it} in the lower half of the SiC band gap (see figure 11), may be explained by a reduced carbon supply rate (directly related to the SiC oxidation rate) and/or by formation of compact CN molecules which, because of their size, may provide an additional pathway for carbon out-diffusion from the SiC/oxide interface [91]. Finally, one more mechanism perhaps of importance in explaining the benign effect of nitridation of the oxide in SiC/SiO_2 structures may be the suppression of the lateral transport of elemental carbon at the interface, required for C cluster formation.

5. Conclusions

The reviewed results suggest that there are no major differences between the SiC/SiO_2 and Si/SiO_2 interface transitions, with the fundamental spectrum of electron states, pertaining to

bulk material, established in both cases within subnanometre distances from the interface plane. The high density of SiC/SiO_2 interface traps appears mainly related to the influence of two factors: clustering of carbon at the interface and the presence of intrinsic defects in the near-interfacial oxide layers. The energy levels of these oxide defects enter the band gap in the wide-band-gap SiC polytypes (e.g., 4H-SiC). These two dominant contributions of interface states to D_{it} exhibit a broad energy distribution due to statistical variation of the carbon cluster size and the random surrounding of defects in the oxide. However, both appear structurally well defined, which may offer possibilities for their successful elimination. The recent results on the reduction of the SiC/SiO_2 interface state density support the view that there are no fundamental limitations that would eclipse the realization of device-grade SiC MOS characteristics.

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